Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 13. (Cancelled)

14. (Original) A semiconductor integrated circuit comprising:

an aging circuit configured by parallel-connecting a plurality of aging devices in which an age-based change occurs while a power supply is disconnected, and an output signal sensed in read changes over time; and

a sense circuit comparing the output signal from the aging circuit with a reference signal.

15. (Original) The circuit according to claim 14, wherein when a time until an output signal from each of the aging devices reaches a predetermined level is defined as a life time of each of the aging devices and a time until the output signal from the aging circuit reaches a level of the reference signal is defined as a life time of the aging circuit, the level of the reference signal is so set as to make the life time of the aging circuit longer than an average life time of the aging devices.

16. (Original) The circuit according to claim 14, wherein a level of the reference signal is set to a value smaller by a predetermined offset amount than a value at which the output signal from the aging circuit is maximized upon a lapse of a time, or a value larger by a predetermined offset amount than a value at which the output signal from the aging circuit is minimized upon a lapse of a time.

17. (Original) The circuit according to claim 14, which further comprises a memory that stores the reference signal, and in which a level of the reference signal stored in the memory is adjusted to control a life time of the aging circuit.

18. (Original) The circuit according to claim 14, wherein the aging device has a charge accumulation layer accompanied by leakage while the power supply is disconnected.

19. (Original) The circuit according to claim 14, wherein the aging device is configured by series-connecting a plurality of field effect devices each having a charge accumulation layer accompanied by leakage while the power supply is disconnected.

20. (Original) The circuit according to claim 14, wherein

the aging circuit comprises a first sub-aging circuit configured by parallel-connecting a plurality of first aging devices in which the output signal decreases over time, and a second sub-aging circuit configured by parallel-connecting a plurality of second aging devices in which the output signal increases over time,

the first sub-aging circuit and the second sub-aging circuit are series-connected, and

when a time until the output signal from the first sub-aging circuit reaches a first predetermined level is defined as a life time of the first sub-aging circuit and a time until the second sub-aging circuit reaches a second predetermined level is defined as a life time of the second sub-aging circuit, the life time of the first sub-aging circuit is longer than the life time of the second sub-aging circuit.

21. (Original) The circuit according to claim 14, wherein

the aging circuit comprises a first sub-aging circuit configured by parallel-connecting a plurality of first aging devices in which the output signal decreases over time, and a second sub-aging circuit configured by parallel-connecting a plurality of second aging devices in which the output signal increases over time,

the first sub-aging circuit and the second sub-aging circuit are parallel-connected, and

when a time until the output signal from the first sub-aging circuit reaches a predetermined level is defined as a life time of the first sub-aging circuit and a time until the second sub-aging circuit reaches the predetermined level is defined as a life time of the second sub-aging circuit, the life time of the first sub-aging circuit is shorter than the life time of the second sub-aging circuit.

22. (Original) The circuit according to claim 14, further comprising a memory area where correspondence codes of the output signal from the aging circuit and lapsed times are stored in advance, and

the sense circuit compares the output signal from the aging circuit with the correspondence codes stored in the memory area, and senses a lapsed operation time of the aging circuit.

23. (Original) The circuit according to claim 14, wherein the aging circuit comprises N sub-aging circuits each having a different life time from others defined by a time until an added output signal within each of the N sub-aging circuits reaches a predetermined reference signal set for each of the N sub-aging circuits, and

the sense circuit compares the added output signal from each of the N sub-aging circuits with the predetermined reference signal, and senses whether or not each of the N sub-aging circuit closes a life time thereof.

24. (Original) The circuit according to claim 23, wherein

each of the N sub-aging circuits has the different life time from others by a predetermined time which is obtained by dividing, by N, a difference between the shortest life time and the longest life time among the N sub-aging circuits, and

the sense circuit senses a lapsed operation time of the aging circuit by sensing each of the life times of the N sub-aging circuits.

25. - 31 (Cancelled).